

Application Serial Number 10/517,471
Response to Office Action
Dated May 16, 2007

REMARKS / DISCUSSION OF ISSUES

Claims 1-9 are pending. Claims 1 and 4 are independent claims.

Unless indicated to the contrary, claims are amended to delete European-style phraseology and not for statutory reasons.

As the improper multiple dependencies are eliminated, full consideration and examination of claims 7-10 is requested.

Rejections under 35 U.S.C. § 102

Claims 1-6 were rejected as being anticipated by *Sheldon, et al.* (U.S. Patent 6,307,480). For at least the reasons set forth herein, Applicants respectfully submit that this rejection is improper and should be withdrawn.

At the outset Applicants rely at least on the following standards with regard to proper rejections under 35 U.S.C. § 102. Notably, a proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen*, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

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Sheldon, et al. fails to disclose at least one feature of claim 1 and claim 4

Claim 4 is drawn to a base chip adapted to monitor operation of at least one microcontroller unit and features:

"at least one reset unit connected to the microcontroller unit, and adapted to reset the microcontroller unit, and at least one monitoring module that is associated with the microcontroller unit and to which the fact that a reset of the microcontroller unit has taken place can be acknowledged by at least one confirming signal wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both."

Claim 1 is drawn to a method and includes similar features.

As such, as amended, claims 1 and 4 feature that the *confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.* In the Office Action, the Examiner directs Applicants to column 4, lines 34-44 of *Sheldon, et al.* for the alleged disclosure of these features. Applicants have reviewed the noted portion of the reference and respectfully submit that these features are not disclosed therein. Specifically, column 4, lines 34-44 discloses:

If the battery monitor 20 is generating a low dead battery signal 28, current will flow from V_{cc} through R_p and through the parallel combination of R_{S2} and R_L . The value of R_{S2} is chosen to assure that the resistor divider created by R_p and the parallel combination of R_{S2} and R_L causes a low reset signal 44, indicating that a reset is requested. Further, the value of C_L is chosen such that the time constant of the discharge of C_L is smaller than the duration of the time out signal 26 to assure that the reset signal 44 will arrive at a low level before MN2 is turned off.

The sequence described relates to the request for a reset and receipt of the reset signal before a FET (MN2) is turned off. There is no description of a *confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.*

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For at least the reasons set forth above, the applied art fails to disclose at least one feature of each of claims 1 and 4. Therefore these claims are patentable over the applied art.

Conclusion


In view the foregoing, applicant(s) respectfully request(s) that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees, including, but not limited to, the fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted on behalf of:

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Date: November 16, 2007

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